IN THE CLAIMS

1 (previously presented): A semiconductor device structure, comprising:

a PMOS device and an NMOS device disposed on a substrate,

the PMOS device including a compressive layer inducing a compressive stress in an active region of the PMOS device in a direction longitudinal to a current direction,

the NMOS device including a tensile layer inducing a tensile stress in an active region of the NMOS device in a direction longitudinal to the current direction, wherein

the compressive layer includes a first dielectric material, the tensile layer includes a second dielectric material, and the PMOS and NMOS devices are FinFET devices.

2 (original): The semiconductor device as claimed in claim 1, wherein the first dielectric material comprises SiN.

3 (original): The semiconductor device as claimed in claim 1, wherein the second dielectric material comprises SiN.

4 (original): The semiconductor device structure as claimed in claim 1, wherein the first dielectric material has a substantially uniform compressive stress in a range of -300 MPa to -3000 MPa.

5 (original): The semiconductor device structure as claimed in claim 1, wherein the first dielectric material has a substantially uniform thickness in a range of 200Å to 2000Å.

6 (original): The semiconductor device structure as claimed in claim 1, wherein the second dielectric material has a substantially uniform tensile stress in a range of +200 MPa to +2000 MPa.

7 (original): The semiconductor device structure as claimed in claim 1, wherein the second dielectric material has a substantially uniform thickness in a range of 200Å to 2000Å.

8 (original): The semiconductor device structure as claimed in claim 1, wherein the first dielectric material and the second dielectric material are SiN.

9-17 (cancelled)